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EXAMINER

NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
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2823

NOTIFICATION DATE	DELIVERY MODE
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01/04/2010

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

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DETAILED ACTION

Remarks

1. The Amendment filed on September 25th, 2009 is acknowledged. By this amendment, claims 9 and 10 have been amended. Accordingly, claims 7-19 are currently pending in this application and claims 1, 9, 10, 13, 14 and 15 are in independent form.

Claim Rejections - 35 USC § 103

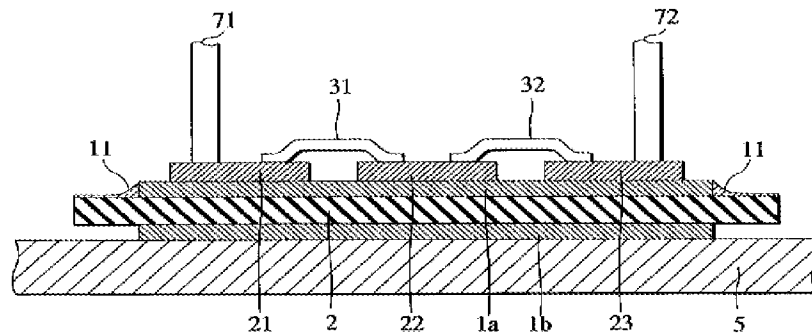
2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
3. Claims 7, 8, 13, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent 6,201,696) in view of Nidan et al. (U.S. Pub. 2002/0005072), both of record.

In re claim 7, **Shimizu et al.** disclose a power semiconductor module, comprising: an electrically insulating substrate **2**; a first electrically conductive layer **1a** disposed on at least one portion of a top surface of said electrically insulating substrate **2**, so as to selectively expose at least one peripheral top region of said electrically insulating substrate **2** (see col. 11, line 56 to col. 12, line 8 and FIG. 2A, for example);

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peripheral region of said electrically insulating substrate **2** is concave-shaped (see col. 12, line 63 to col. 13, line 12 and FIG. 2B, for example).

FIG.2B

However, **Shimizu et al.** is silent about wherein the first electrically insulating material is a polyimide.

Nidan et al. disclose wherein the electrically insulating material is composed of epoxy resin, polyimide resin or the like (see page 3, paragraph [0070]).

As **Nidan et al.** disclosed, one of ordinary skill in the art would have been motivated to substitute polyimide resin for epoxy resin because epoxy resin and polyimide are interchangeable. As known to one of ordinary skill in the art, thermosetting resin such as epoxy or polyester resin serve similar purpose as a thermoplastic resin such as polyimide resin.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Shimizu et al. reference with an electrically insulating material composed of polyimide resin

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as taught by Nidan et al. since epoxy resin and polyimide resin are interchangeable in order to obtain the same result.

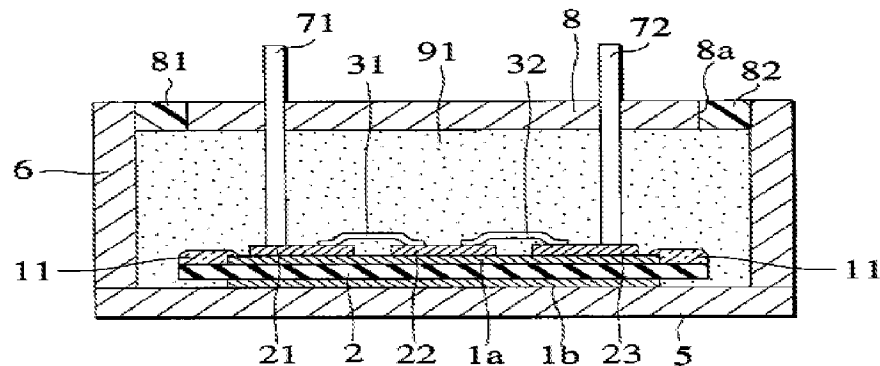
In re claim 8, as applied to claim 7 above, Shimizu et al. in combination with Nidan et al. discloses all claimed limitations including the limitation wherein the electrically insulating substrate **2** is mounted on a bottom plate **5** (see col. 12, lines 9-13 and FIG. 2A, for example).

In re claim 13, Shimizu et al. disclose a power semiconductor module, comprising: an electrically insulating substrate **2**; a first electrically conductive layer **1a** disposed on at least one portion of a top surface of said electrically insulating substrate **2**, so as to selectively expose at least one peripheral top region of said electrically insulating substrate **2** (see col. 11, line 56 to col. 12, line 8 and FIG. 2A, for example);

at least one semiconductor power chip **21/23** mounted on said first electrically conductive layer **1a** (see col. 12, lines 6-8);

a first electrically insulating material **11** disposed in a corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** ((see col. 12, lines 49-58 and FIG. 2A) and (col. 12, line 63 to col. 13, line 12 and FIG. 2B));

FIG. 2A

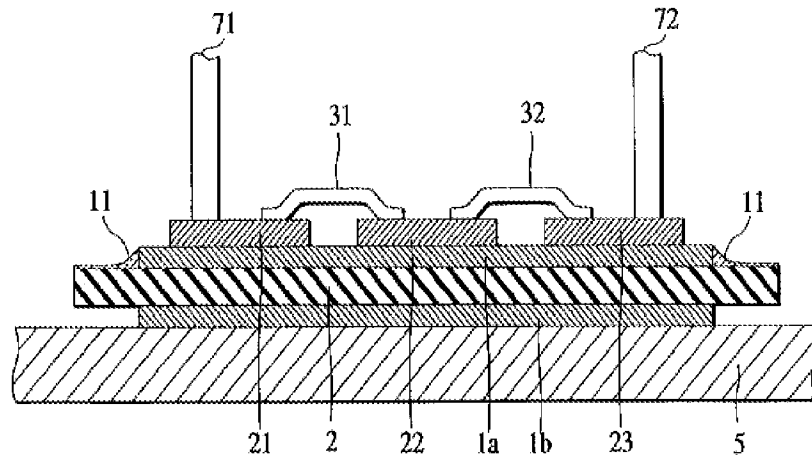


a second insulating material **91** at least partially embedding said semiconductor power chip **21/23**, said electrically insulating substrate **2**, said first electrically conductive layer **1a**, and said first electrically insulating material **11** (col. 11, lines 58-62 and FIG. 2A, for example);

wherein the first electrically insulating material **11** is an epoxy resin or polyester resin (col. 12, lines 49-58), and

the surface of the first electrically insulating material **11** disposed in the corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** is concave-shaped (see col. 12, line 63 to col. 13, line 12 and FIG. 2B, for example),

FIG.2B



wherein the first electrically insulating material **11** fills gaps in a junction between the first electrically conductive layer **1a** and the electrically insulating substrate **2** (see col. 12, lines 49-63 and FIG. 2A).

However, **Shimizu et al.** is silent about wherein the first electrically insulating material is a polyimide.

Nidan et al. disclose wherein the electrically insulating material is composed of epoxy resin, polyimide resin or the like (see page 3, paragraph [0070]).

As **Nidan et al.** disclosed, one of ordinary skill in the art would have been motivated to substitute polyimide resin for epoxy resin because epoxy resin and polyimide are interchangeable. As known to one of ordinary skill in the art, thermosetting resin such as epoxy or polyester resin serve similar purpose as a thermoplastic resin such as polyimide resin.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Shimizu et al. reference with an electrically insulating material composed of polyimide resin as taught by **Nidan et al.** since epoxy resin and polyimide resin are interchangeable in order to obtain the same result.

In re claim 16, as applied to claim 7 above, **Shimizu et al.** in combination with **Nidan et al.** discloses all claimed limitations including the limitation wherein the first electrically insulating material has a low viscosity (see page 3, paragraph [0070] of Nidan et al.).

In re claim 18, as applied to claim 13 above, **Shimizu et al.** in combination with **Nidan et al.** discloses all claimed limitations including the limitation wherein the first electrically insulating material has a low viscosity (see page 3, paragraph [0070] of Nidan et al.).

4. Claims 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent 6,201,696) in view of Nidan et al. (U.S. Pub. 2002/0005072), both of record, as applied to claims 7, 16, 13, and 18 above, and further in view of Sakamoto et al. (U.S. Pub. 2004/0014317), newly discovered.

In re claim 17, as applied to claim 16, Paragraph 3 above, **Shimizu et al.** in combination with **Nidan et al.** disclose all the claimed limitations including wherein the first electrically insulating material has a predetermined viscosity range (see page 3, paragraph [0070] of Nidan et al.).

However, neither **Shimizu et al.** nor **Nidan et al.** specifically disclose that the first electrically insulating material has a viscosity η such that $\eta \leq 1.0 \text{ Pa}\cdot\text{s}$.

Sakamoto et al. disclose an electrically insulating material 41 fills gap in a junction between IC chip 20 and UV tape 40 wherein the first electrically insulating material 41 is a polyimide resin having a viscosity η ranging from 0.1 to 50 Pa·s (see page 25, paragraph [0453] and FIG. 53(D)).

As **Sakamoto et al.** disclosed, one of ordinary skill in the art would have been motivated to provide a first electrically insulating material (polyimide resin) having a viscosity η such that $\eta \leq 1.0 \text{ Pa}\cdot\text{s}$ in order to seal the electronic components so as to protect the electronic components (see page 1, paragraph [0007] of Sakamoto et al.). As known to one of ordinary skill in the art, polyimide resin is preferred to be used for sealing and filling gaps between electronic components because of its viscosity stability, long-term preservability and moisture resistance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify **Shimizu et al.** and **Nidan et al.** references with the polyimide resin of low viscosity η (0.1 to 50 Pa·s) as taught by **Sakamoto et al.** in order to seal the electronic components so as to protect the electronic components (see page 1, paragraph [0007] of Sakamoto et al.) and furthermore, polyimide resin is preferred to be used for sealing and filling gaps between electronic components because of its viscosity stability, long-term preservability and moisture resistance.

Allowable Subject Matter

5. Claims 9, 10, 14 and 15 are allowed over prior art of record.
6. Claims 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons For Allowance

7. The following is an examiner's statement of reasons for allowance:

It is determined that the prior art of record neither anticipates nor renders obvious the claimed subject matter of claims 9 and 10 as a whole taken alone or in combination, in particular, prior art of record does not teach "wherein at least one second electrically conductive layer is disposed between the bottom plate and at least one portion of a bottom surface of the electrically insulating substrate, so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate and wherein a third insulating material is disposed in a second corner formed by the second electrically conductive layer and the peripheral bottom region of the electrically insulating substrate", as recited in independent claim 9, and "wherein a rigid layer of resin is provided between the second electrically insulating material and the semiconductor chip, the substrate, the first conductive layer and the first electrically insulating material", as recited in independent claim 10.

Claims 14-15 are allowed for the same ground that was set forth in Paragraphs 5 and 6 of the Office Action that was mailed on March 19th, 2008.

Claims 11-12 were previously indicated as objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (see Office Action mailed on March 19th, 2008).

Response to Applicants' Amendment and Arguments

8. Applicants' arguments filed on September 25th, 2009 have been fully considered but they are not persuasive.

Applicants contend that the references, Shimizu et al. (U.S. Patent 6,201,696) in view of Nidan et al. (U.S. Pub. 2002/0005072), herein known as **Shimizu** and **Nidan** fails to disclose or suggest a first electrically insulating material disposed between an electrically insulating substrate and a first electrically conductive layer and in a corner region formed by the first electrically conductive layer and a peripheral region of the electrically insulating substrate.

Applicants further contend that "Applicants put forward that one of ordinary skill would not have looked to Nidan in an effort to remedy the deficiencies of Shimizu because the functional characteristics of the resin member as applied in Nidan are not transferable to the device described in Shimizu.

In response to Applicants' contention that **Shimizu** and **Nidan** do not disclose or suggest a first electrically insulating material disposed between said electrically insulating substrate and said electrically conductive layer as required by the Applicants' claimed invention, Examiner respectfully disagrees.

Applicants' attention is respectfully directed to ((col. 12, lines 49-58 and FIG. 2A) and (col. 12, line 63 to col. 13, line 12 and FIG. 2B)) where **Shimizu** discloses a first electrically insulating material **11** disposed in a corner region formed by said first electrically conductive layer **1a** and said peripheral region of said electrically insulating substrate **2** ((see col. 12, lines 49-58 and FIG. 2A) and (col. 12, line 63 to col. 13, line 12 and FIG. 2B)). But **Shimizu** is silent about providing a first electrically insulating material **11** disposed between said electrically insulating substrate **2** and the first electrically conductive layer **1a**.

However, the secondary reference, **Nidan**, discloses wherein the electrically insulating material is composed of epoxy resin, polyimide resin or the like (see page 3, paragraph [0070]).

As **Nidan et al.** disclosed, it is respectfully submitted that one of ordinary skill in the art would have been motivated to substitute polyimide resin as taught by **Nidan** for epoxy resin of **Shimizu** because **Nidan** provides clear evidence that epoxy resin and polyimide are interchangeable. As known to one of ordinary skill in the art, thermosetting resin such as epoxy or polyester resin serves similar purpose as a thermoplastic resin such as polyimide resin.

Therefore, it is respectfully submitted that it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to modify **Shimizu et al.** reference to replace **Shimizu**'s epoxy resin with an electrically insulating material composed of polyimide resin as taught by **Nidan et al.** since epoxy resin and polyimide resin are interchangeable in order

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to obtain the same result (having the first electrically insulating material such as polyimide resin disposed between said electrically insulating substrate and said first electrically conductive layer because it is well-known to one having ordinary skill in the art that polyimide resin material has lower viscosity and thus it is capable of creeping into gap that exist between the electrically insulating substrate and the first electrically conductive layer).

For this reason, Examiner holds the rejection proper.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the

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examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khiem D. Nguyen/
Primary Examiner, Art Unit 2823
December 24th, 2009